Abstracts

Custom hardware implementation of the finite-difference time-domain (FDTD) method

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Finite-Difference Time-Domain (FDTD) Analysis is a very popular method for solving electromagnetic problems. The algorithm is computationally Intensive and simulations can take several days to run on traditional, multiprocessor supercomputer platforms. Reducing the runtime of these simulations, by an order of magnitude or more, would greatly increase the productivity of FDTD users and open new avenues of research. A hardware implementation of a one-dimensional FDTD computational cell is presented, with the goal of accelerating three-dimensional computations by a factor of 10-100 times. A free-space, cavity resonator Is used to successfully verify the FDTD simulation on hardware. Computational speed is very promising and is independent of the number of cells in the simulation. Larger simulations require more hardware. A typical simulation size (100/spl times/100/spl times/100) is hardware prohibitive, so future work will Investigate hardware sharing methods.

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